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10/563,285

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EXAMINER

WILLIS, RANDAL L

ART UNIT

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	<b>Application No.</b> 10/563,285	<b>Applicant(s)</b> KIDA ET AL.	
	<b>Examiner</b> RANDAL WILLIS	<b>Art Unit</b> 2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 14 December 2010.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-6 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-6 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892)                     | 4) <input type="checkbox"/> Interview Summary (PTO-413)           |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____                                      |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)          | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____  | 6) <input type="checkbox"/> Other: _____                          |

### **DETAILED ACTION**

1. This office action is in response to application 10/563285 filed January 3<sup>rd</sup> 2006.

Claims 1-6 are currently pending and have been examined.

### ***Response to Arguments***

2. Applicant's arguments with respect to claims 1-6 have been considered but are not persuasive. Applicant argues Edwards uses a single sample line to turn transistors T2 and T3 on/off, forcing them to be in the same logic state. However, the claim language makes no mention of circuit timings in which T2 or T3 is turned on while the other is turned off, therefore the timing of Edwards can read upon the invention as claimed. Applicant's argument that Edwards outputs directly to the column is correct, however the secondary reference Yamazaki teaches this limitation, which is a well known use of buffers in the art.  
  
Applicant argues for claim 3 that Edwards and Yamazaki fail to disclose the buffer and Digital to Analog converter of the claimed invention. However, Yamazaki clearly states in [0110] the inclusion of both buffer circuits and D/A converters in the source driver, the structure and function of which is well known in the art and within the skill of one of ordinary skill in the art at the time of the invention to incorporate into the display device of Edwards.

***Claim Rejections - 35 USC § 103***

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

4. Claims 1-6 rejected under 35 U.S.C. 103(a) as being unpatentable over Edwards in view of Yamazaki (2006/0267899).

Apropos claim 1, Edwards teaches:

A method for operating a constant current circuit comprising,

after connecting a sampling capacitor (72, Fig. 8) connected between a gate and a source of a first transistor (capacitor 72 connected between gate of source transistor T4, Fig. 8) and a drain of the first transistor to a reference current source (T4 connected to current source 40, Fig. 8) and setting a voltage across the sampling capacitor to a

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voltage between the gate and the source produced while the first transistor is driven by a reference current of the reference current source (Col 8 line 60 through Col 9 lines 5),

cutting off the connection among the sampling capacitor, the first transistor and the reference current source, as well as connecting the drain of the first transistor to a driving target (Col 9 lines 1-10), and driving the driving target by a current of first the transistor due to the voltage between the gate and the source that is set in the sampling capacitor (Col 9 lines 1-10)

wherein said cutting off the connection comprises applying a first signal (sample, Fig. 9) to a gate of a second transistor (T2, Fig. 8) connected between the drain of the first transistor and the reference current source (T2 between T4 and current source 40)

a second signal to a gate of a third transistor connected between the gate and drain of the first transistor (Sample applied to gate of T3, which is between the gate and drain of T4)

a third signal (Output Enable, Fig. 9) to a gate of a fourth transistor (T5, Fig. 8) connected between the drain of the first transistor and the driving target.

However, Edwards fails to explicitly teach:

The second signal is the logical inverse of said first signal.

However, one of ordinary skill in the art at the time of the invention would realize that the logical value of the signal applied to the gate of the transistor is a function of whether the transistor should be turned on or off and the type of transistor used. There are only a finite number of configurations the transistors can be in, either both are NMOS, both are PMOS or one is NMOS and the other PMOS. Therefore it would have

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been obvious to one of ordinary skill in the art at the time of the invention to try the three possible configurations, in which using both a NMOS for one of T3 and T2 and using a PMOS transistor for the other of T3 and T2 would necessitate the use of inverted first and second signals to achieve the driving method put forth by Edwards.

Wherein said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit during the precharge period (Fig. 11 shows the capacitor is charged prior to the output enable being applied and can be considered a pre-charge period).

However Edwards fails to explicitly teach:

a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;

the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor;

in the same field of flat panel displays, Yamazaki teaches a source driver circuit which outputs to a buffer circuit to provide the data to the data lines ([0110]).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known method of having the driver output to buffers in the data driver as taught by Yamazaki in the display of Edwards in order to provide the predictable result of steady analog signals to be able to charge the capacitor to the correct voltage for displaying an image.

Apropos claim 2, Edwards teaches:

further comprising repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target (Inherent in active matrix displays to repeat driving periods to display images).

Apropos claim 3, Edwards teaches:

A flat display device constructed so that a display section made of pixels arranged in a matrix form (Fig. 1), a vertical driving circuit for sequentially selecting the pixels of the display section through gate lines (16, Fig. 1), and a horizontal driving circuit for driving pixels selected through the gate lines (18, Fig. 1), by signal lines of the display section,

characterized in that:

the horizontal driving circuit comprises:

after connecting a sampling capacitor (72, Fig. 8) connected between a gate and a source of a transistor (capacitor 73 connected between gate of source of transistor T4, Fig. 8) and a drain of the transistor to a reference current source (T4 connected to current source 40, Fig. 8) and setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the transistor is driven by a reference current of the reference current source (Col 8 line 60 through Col 9 lines 5),

cutting off the connection among the sampling capacitor, the transistor and the reference current source, as well as connecting the drain of the transistor to a driving target (Col 9 lines 1-10), and driving the driving target by a current of the transistor due to the voltage between the gate and the source that is set in the sampling capacitor (Col 9 lines 1-10)

wherein said cutting off the connection comprises applying a first signal (sample, Fig. 9) to a gate of a second transistor (T2, Fig. 8) connected between the drain of the first transistor and the reference current source (T2 between T4 and current source 40)

a second signal to a gate of a third transistor connected between the gate and drain of the first transistor (Sample applied to gate of T3, which is between the gate and drain of T4)

a third signal (Output Enable, Fig. 9) to a gate of a fourth transistor (T5, Fig. 8) connected between the drain of the first transistor and the driving target.

However, Edwards fails to explicitly teach:

The second signal is the logical inverse of said first signal.

However, one of ordinary skill in the art at the time of the invention would realize that the logical value of the signal applied to the gate of the transistor is a function of whether the transistor should be turned on or off and the type of transistor used. There are only a finite number of configurations the transistors can be in, either both are NMOS, both are PMOS or one is NMOS and the other PMOS. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to try the three possible configurations, in which using both a NMOS for one of T3 and T2 and using a



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PMOS transistor for the other of T3 and T2 would necessitate the use of inverted first and second signals to achieve the driving method put forth by Edwards.

However Edwards fails to explicitly teach:

a digital-to-analog conversion circuit for performing digital-to-analog conversion processing of gradation data indicative of gradations of the pixels; and

a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;

the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor;

in the same field of flat panel displays, Yamazaki teaches a source driver circuit which contains a D/A converter and a buffer circuit to provide the data to the data lines ([0110]).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known method of having D/A converters and buffers in the data driver as taught by Yamazaki in the display of Edwards in order to provide the predictable result of steady analog signals to be able to charge the capacitor to the correct voltage for displaying an image.

Apropos claim 4, Edwards teaches:

The flat display device according to claim 3, wherein the constant current circuit is configured for repeating a period for setting the voltage across the sampling capacitor and a period for driving the driving target (Inherent in active matrix displays to repeat

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driving periods to display images), the period for setting the voltage across the sampling capacitor being set as a period for precharge of the display section (Fig. 9 shows capacitor is charged prior to the output being enabled which would drive the display pixel).

Apropos claim 5, Edwards teaches:

A constant current circuit, comprising:

A transistor having a gate, a source, and a drain (T4, Fig. 10), the drain of the transistor being configured for selective connection to a reference current source (Connected to reference 40 through T2, Fig. 10); and

A sampling capacitor (72, Fig. 10) configured for selective connection between the gate and the source of the transistor (T4, Fig. 10), for setting a voltage across the sampling capacitor to a voltage between the gate and the source produced while the transistor is driven by a reference current of the reference current source (Col 9 lines 1-5),

Wherein the drain of the transistor is selectively connected to a driving target after setting said voltage across the sampling capacitor, for driving the driving target by a current of the transistor due to the voltage between the gate and the source that is set in the sampling capacitor (output enable T5, Fig. 10 selectively connects T4 to the output column load)

A second transistor having a gate, a source and a drain, the drain of the second transistor being configured to selectively connect the first transistor and the reference current source (T2, connected between T4 and 40, Fig. 10)

Wherein the gate of the second transistor is configured to receive a first signal (sample, Fig. 10) that enables the selective connection of the first transistor and the reference current source;

A third transistor (T3, Fig. 10) having a gate, a source and a drain, the third transistor being configured to set the voltage across the sampling capacitor (T3 allows current to flow from 40 into capacitor 72),

Wherein the gate of the third transistor is configured to receive a second signal (sample, Fig. 10) that enables the setting of the voltage across the sampling capacitor; and

A fourth transistor (T5, Fig. 10) having a gate, a source, and a drain, the fourth transistor being configured to selectively connect the driving target and the drain of the first transistor (T5 positioned between output column and T4, Fig. 10),

Wherein the gate of the fourth transistor is configured to received a third signal (Output enable, Fig. 10) that enables the selective connection of the driving target and the drain of the first transistor.

Wherein said setting the voltage across the sampling capacitor and said cutting off the connection occur within a precharge period to cause the constant current circuit to be temporarily connected to a source of a buffer circuit transistor of the buffer circuit

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during the precharge period (Fig. 11 shows the capacitor is charged prior to the output enable being applied and can be considered a pre-charge period).

However, Edwards fails to explicitly teach:

The second signal is the logical inverse of said first signal.

However, one of ordinary skill in the art at the time of the invention would realize that the logical value of the signal applied to the gate of the transistor is a function of whether the transistor should be turned on or off and the type of transistor used. There are only a finite number of configurations the transistors can be in, either both are NMOS, both are PMOS or one is NMOS and the other PMOS. Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to try the three possible configurations, in which using both a NMOS for one of T3 and T2 and using a PMOS transistor for the other of T3 and T2 would necessitate the use of inverted first and second signals to achieve the driving method put forth by Edwards.

However Edwards fails to explicitly teach:

a buffer circuit for driving the signal lines by means of an output signal from the digital-to-analog conversion circuit;

the buffer circuit drives the signal lines by a source follower circuit formed by connecting a constant current circuit to a source of a transistor;

in the same field of flat panel displays, Yamazaki teaches a source driver circuit which outputs to a buffer circuit to provide the data to the data lines ([0110]).

Therefore it would have been obvious to one of ordinary skill in the art at the time of the invention to use the known method of having the driver output to buffers in the

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data driver as taught by Yamazaki in the display of Edwards in order to provide the predictable result of steady analog signals to be able to charge the capacitor to the correct voltage for displaying an image.

Apropos claim 6, Edwards teaches:

Wherein the period for setting the voltage and cutting the connection and a period for driving the buffer circuit are repeated (Inherent in active matrix displays to repeat driving periods to display images).

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of

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the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to RANDAL WILLIS whose telephone number is (571)270-1461. The examiner can normally be reached on Monday to Thursday, 8am to 5pm (EST).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on 571-272-7764. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Alexander S. Beck/  
Supervisory Patent Examiner, Art Unit 2629

RLW